EMI-Optimized Design for the CA-IS2062A Ultra-small, Isolated CAN Transceiver

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1. Introduction

This document is designed to complement the CA-IS2062A data sheet to provide a low-EMI design solution for the isolated CAN transceivers. This application note discusses EMI suppression methods, provides a reference design and the 30MHz to 1GHz frequency range test results according to EN55032(CISPR32) Class-B standard based on a 2-layer board design. Also refer AN001 EMI-Optimized Design for the Isolated Power Supply (AN001.pdf (chipanalog.com)) for more details.

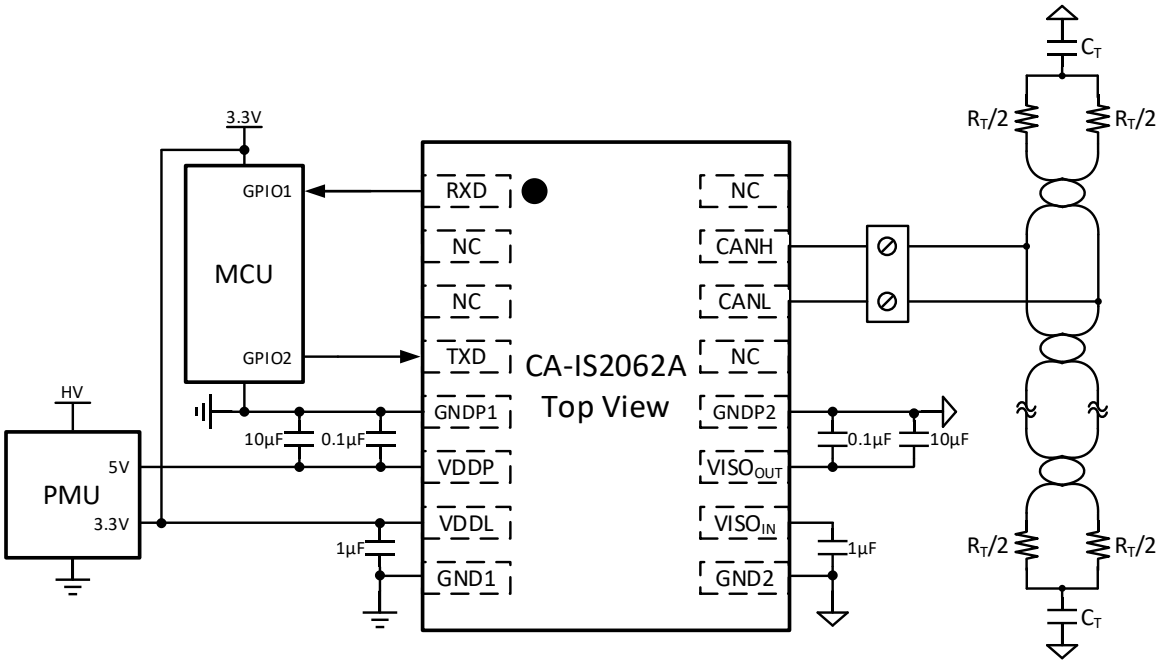

Figure 1-1. Typical application circuit

2. EMI-Optimized Design

2.1. CA-IS2062A General Description

Figure 2-1 shows the CA-IS2062A pin configuration.

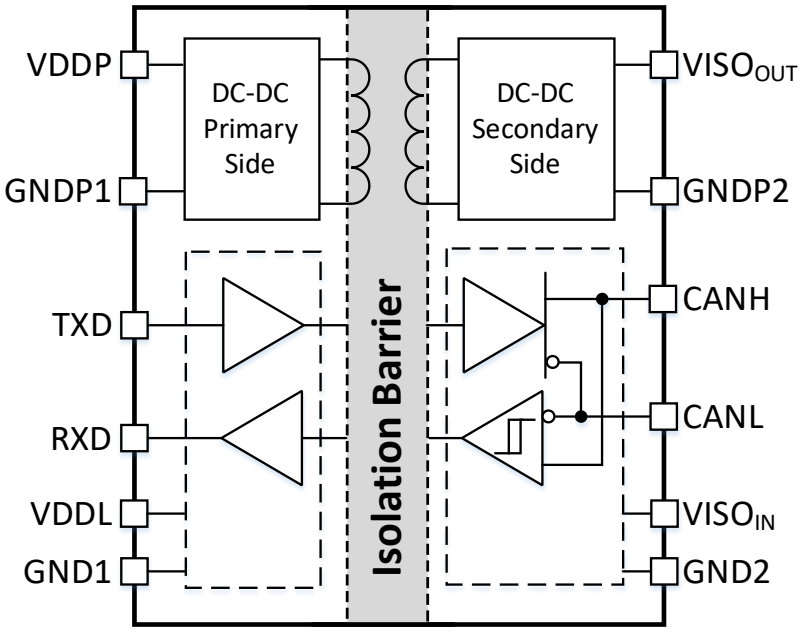

Figure 2-1. CA-IS2062A pin configuration

The CA-IS2062A is an ultra-small (LGA16 package), galvanically-isolated CAN transceiver with a built-in isolated DC-DC converter and transformer, eliminating the need for a separate isolated power supply in space-constrained designs. The main sources of radiation are the high di/dt and dv/dt generated by the high-frequency switching operation of the on-chip transformer. Furthermore, it is important for designers to consider the common-mode noise generated by parasitic components on both the primary and secondary sides.

The CA-IS2062A is designed to operate from a single power supply (VDDP) on the primary side. The integrated DC-DC converter generates a 5V operating voltage for the secondary side, designated $VISO_{OUT}$. Additionally, the CA-IS2062A features an independent logic supply input (VDDL), enabling seamless integration of logic input/output lines with a voltage range of 2.5V to 5.5V. The VDDL pin can be connected to an individual power supply or linked with the VDDP pin for a single supply design.

The following sections provide a comprehensive overview of the measures that can be taken to minimise EMI and reflections in the design of a CA-IS2062A circuit.

2.2. Optimized Design and Layout

2.2.1. Decoupling Capacitor Placement

Careful PCB layout is critical to achieve clean and stable communication operation. To make sure device operation is reliable at all data rates and supply voltages, we recommend to add a minimum 10nF high-frequency bypass capacitor and a bulk energy-storage capacitor in paralleling between VDDP and GNDP1, $VISO_{OUT}$ and GNDP2. Selecting 10nF to 100nF low-ESL/low-ESR MLCC capacitor as the high frequency decoupling capacitor, also this capacitor must be placed closer to VDDP or $VISO_{OUT}$ pin, the maximum distance is within 2mm, to reduce parasitic inductance and current loop. This is very essential for optimized radiated emissions performance, see Figure 2-2 recommended decoupling capacitors placement for the PCB layout.

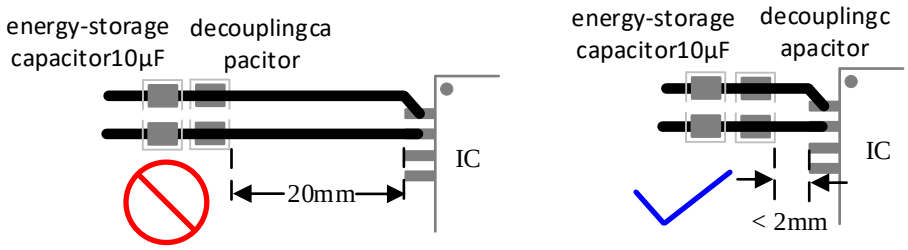

Figure 2-2. Decoupling capacitor placement

2.2.2. Y-capacitor Between Primary-side and Secondary-side

During high-frequency operation, the common-mode current generates a current loop between the parasitic capacitance of the primary and secondary coils, as well as the PCB parasitic capacitance. The larger the loop area, the stronger the radiation generated. It is recommended to place a Y capacitor across the isolation barrier, between the primary-side reference ground (GNDP1) and secondary-side reference ground (GNDP2). The Y-capacitor creates a very short path for the parasitic current return to primary side to reduce the loop area, and reduce the high-frequency radiation from the board, see Figure 2-3.

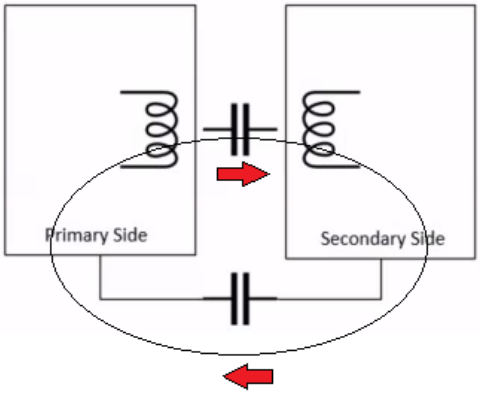

Figure 2-3. Y-capacitor across the isolation barrier

2.2.3. Ferrite Bead/Common-mode Inductor/Differential-mode Inductor

On the primary-side, a pair of ferrite beads with a high frequency impedance of 1KΩ@ 100MHz are placed on the power line and ground line respectively, thereby breaking the path of larger common-mode current loops. This offers further high-frequency attenuation and blocks the switching noise. Place the beads close to the decoupling capacitors as shown in Figure 2-4. Also, a common-mode inductor or/and a differential-mode inductor can be an option based on the EMI test result. In the CA-IS2062A reference design, to reduce low-frequency noise, two differential-mode inductors are added between the input power supply and the primary-side supply inputs. Ground planes must be avoided under these magnetic components to avoid the parasitic capacitance affecting high-frequency attenuation.

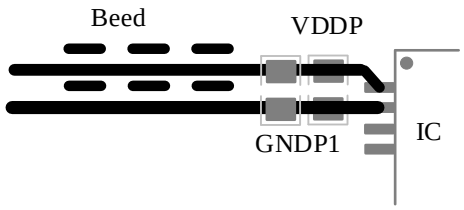

Figure 2-4. Ferrite beads placement

2.2.4. Building the edge guarding

A grounding vias can be added around the PCB to form a via guard ring and to return the noise to the ground to reduce the radiation and interfere to external circuits, as shown in Figure 2-5. If there are more than two rows of vias, the vias placed in the two rows shall be staggered from each other.

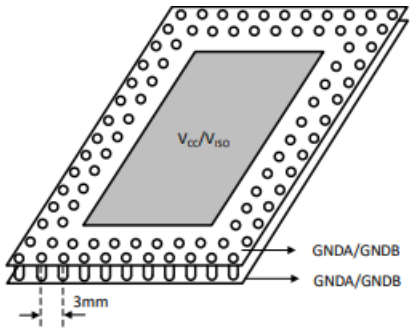

Figure 2-5. Vias guard ring around the edges of ground layers

3. CA-IS2062A Low-EMI Reference Design

3.1. PCB Design Guide

1) It is recommended that decoupling capacitors be placed as close as possible to the device pins, with a maximum distance of less than 2mm. Please refer to Figure 3 1, C3/C4 and C6/C7 for details. With regard to the individual logic supply input VDDL and the power supply input for the cable-side VISOIN, we would like to suggest placing a 0.1μF ceramic capacitor (C5, C8 in Figure 3 1) between VDDL and GND1, $VISO_{IN}$ and GND2, respectively.Place the beads BD1, BD2 and BD3, BD4 close to C3/C4 and C5. Install the differential-mode inductors at L1/ L2 tag;
2) On the bottom layer of the PCB, a Y-capacitor should be placed between GNDP1 and GNDP2. The Y capacitor can be connected to a resistor (RY) with an appropriate resistance, such as 20Ω, in series.
3) The LM1086ISX-ADJ 12V to 5V LDO has been selected on the left of L1/L2 to provide a clean +5V supply for the CA-IS2062A CAN transceiver on the reference design board.

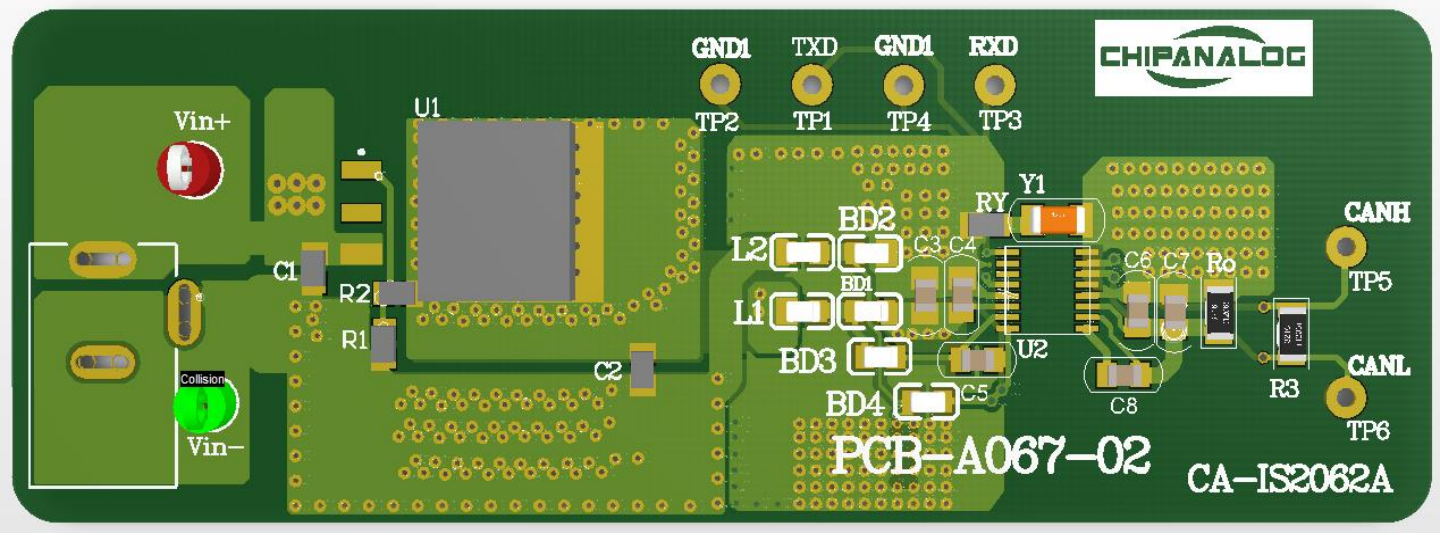

Figure 3-1. CA-IS2062A reference design board

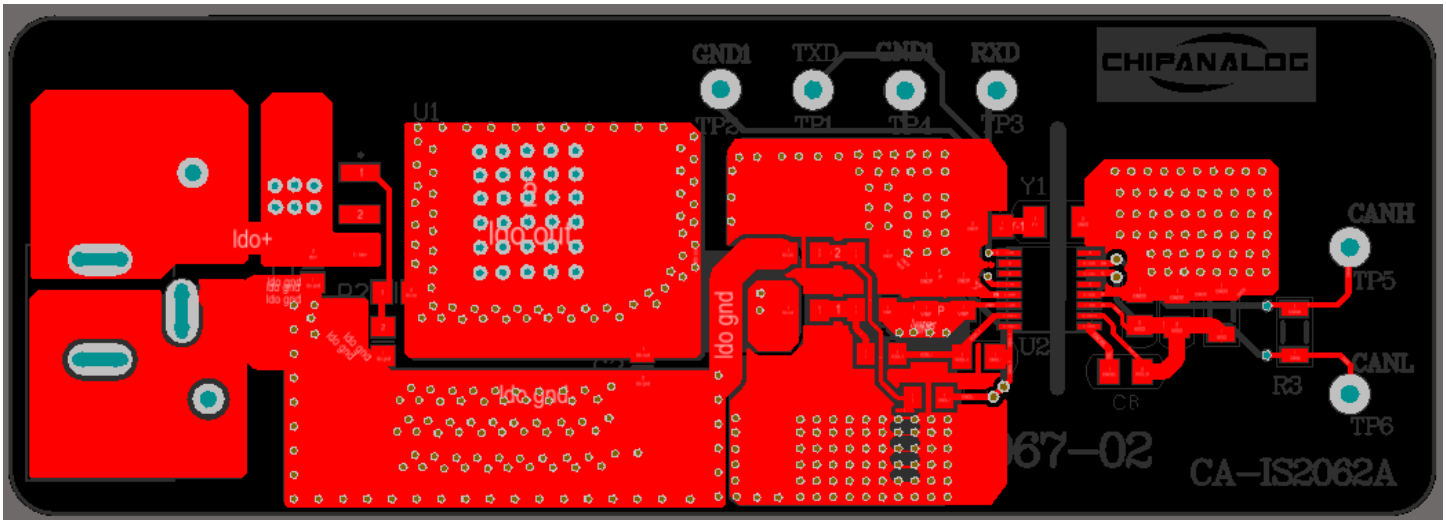

Figure 3-2. Reference design PCB top layer

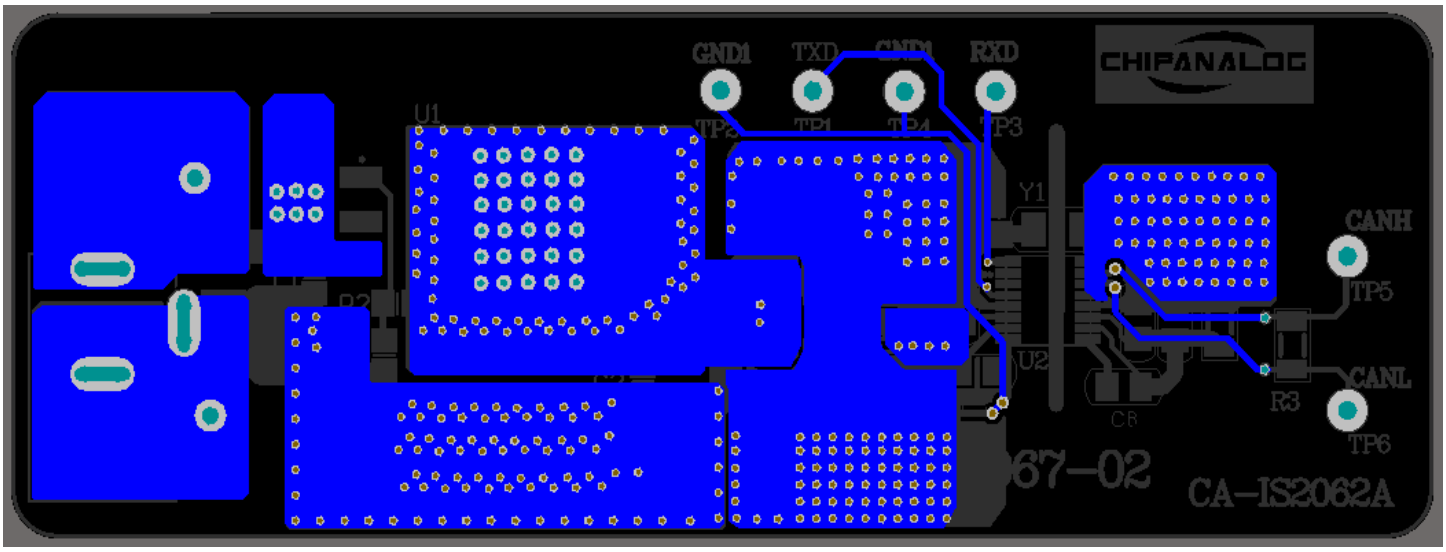

Figure 3-3. Reference design PCB bottom layer

3.2. CA-IS2062A Reference Design Schematic

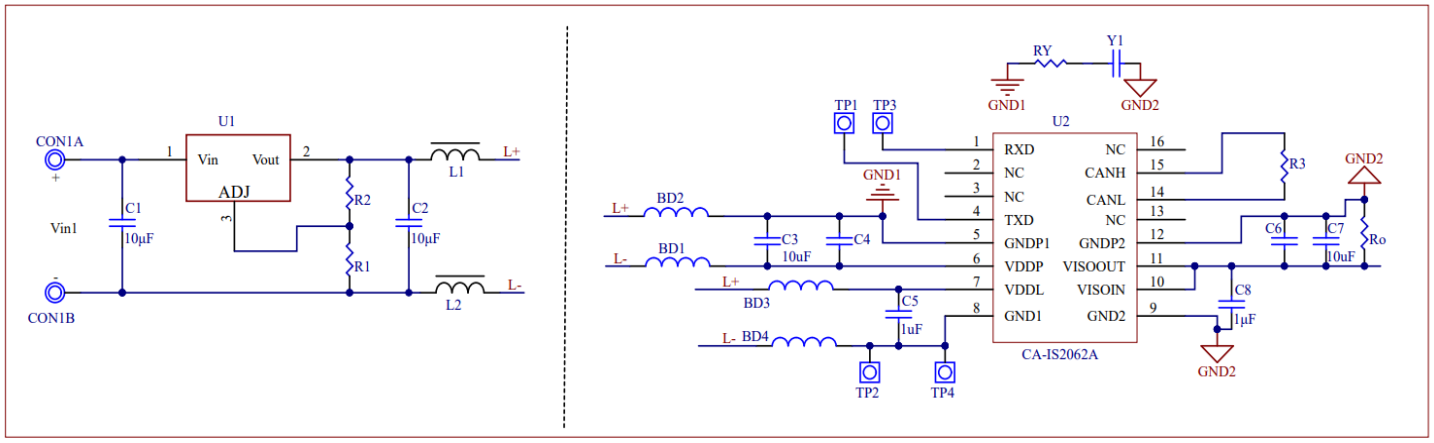

Figure 3-4. CA-IS2062A reference design board schematic

Table 3-1. Component List

Device name	Designation	Spec	Part number	Note
Ferrite bead	BD1, BD 2	1kΩ at 100MHz	BLM18HE102SN1	
Resistor	BD3, BD4	0Ω	0805	
Y capacitor	Y1	33pF	GRM31A7U3D390JW31	
Differential-mode inductors	L1, L2	2.2μH	MLZ2012M2R2HT000	
Resistor	R1	360Ω	0603	
	R2	120Ω	0603	
	R3	60Ω	1206	
	Ro	180Ω	1206	
	RY	20Ω	0805	
Decoupling capacitors	C1	4.7μF/10V	0805	
	C2	10μF/10V	0805	
	C4, C6	10nF/10V	0805	
	C3, C7	10μF/10V	0805	
	C5, C8	1μF/10V	0805	
U1	U1	LDO	LM1086ISX-ADJ, TI	
U2	U2	IC	CA-IS2062A	

Table 3-2. Reference design summary

Board	Design margin	Frequency	PCB-layers	Overlap capacitors	Y-capacitor	Common-mode inductor	Differential-mode inductor
Reference design	3.05dB	198.6MHz	2	N/A	33pF	N/A	2.2μH (2pcs)

3.3. EMI Test Results

The test result is shown in Figure 3-5 and Figure 3-6, this solution meets EN55032(CISPR32) radiated emissions Class B standard, and also leave 3.05dB (horizontal)/4.95dB(vertical) design margin.

Table 3-3. EMI test results summary

LDO Input voltage	$VISO_{OUT}$ output voltage	$VISO_{OUT}$ Load	Design margin	
			vertical	horizontal
12V	5V	5V/180Ω	3.05dB	4.95dB

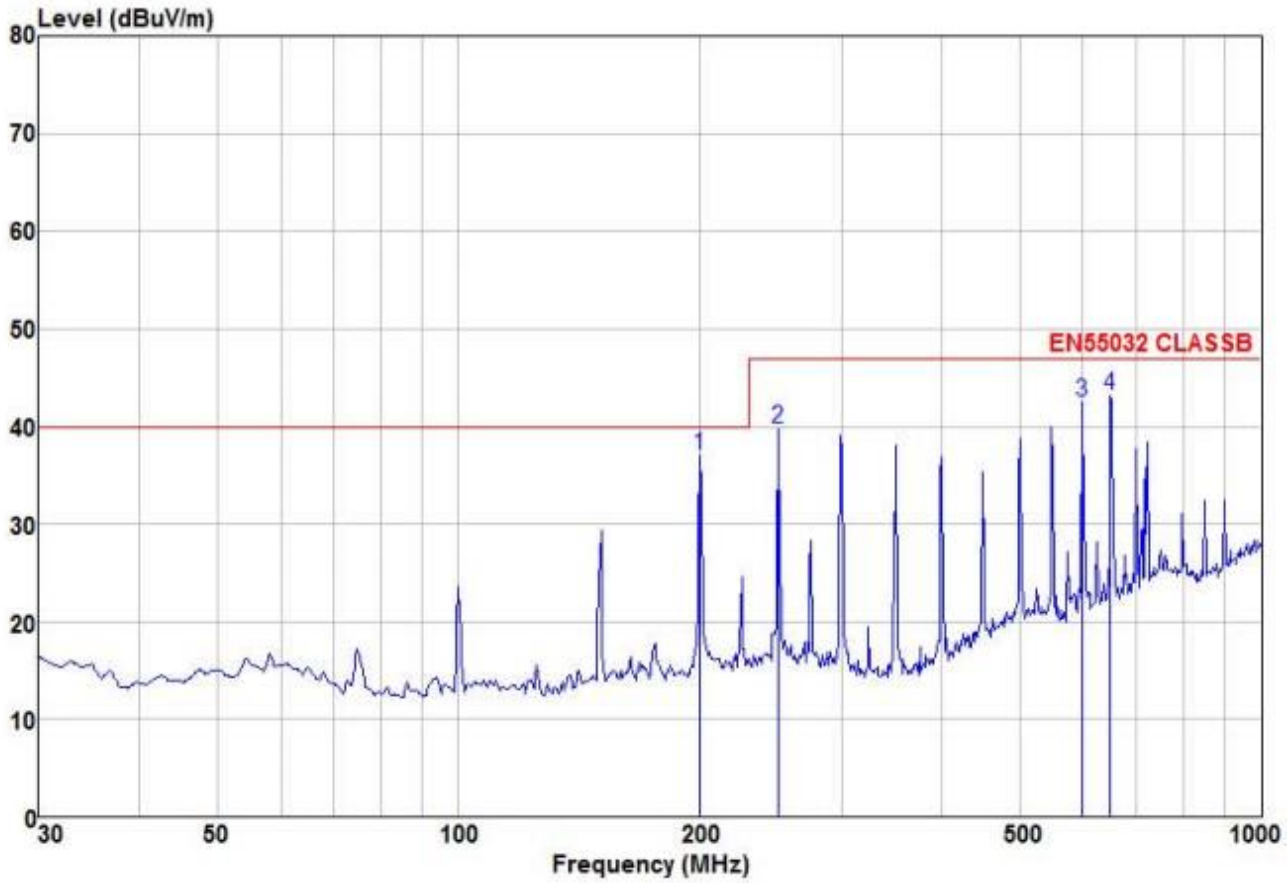

Figure 3-5. Horizontal radiation test result

Test conditions:

1) Input voltage for the reference design board: 12V lead-acid battery;
2) $VISO_{OUT}$ = 5V， Ro = 180Ω.

Test result: 30MHz-1GHz, Margin = 3.05dB.

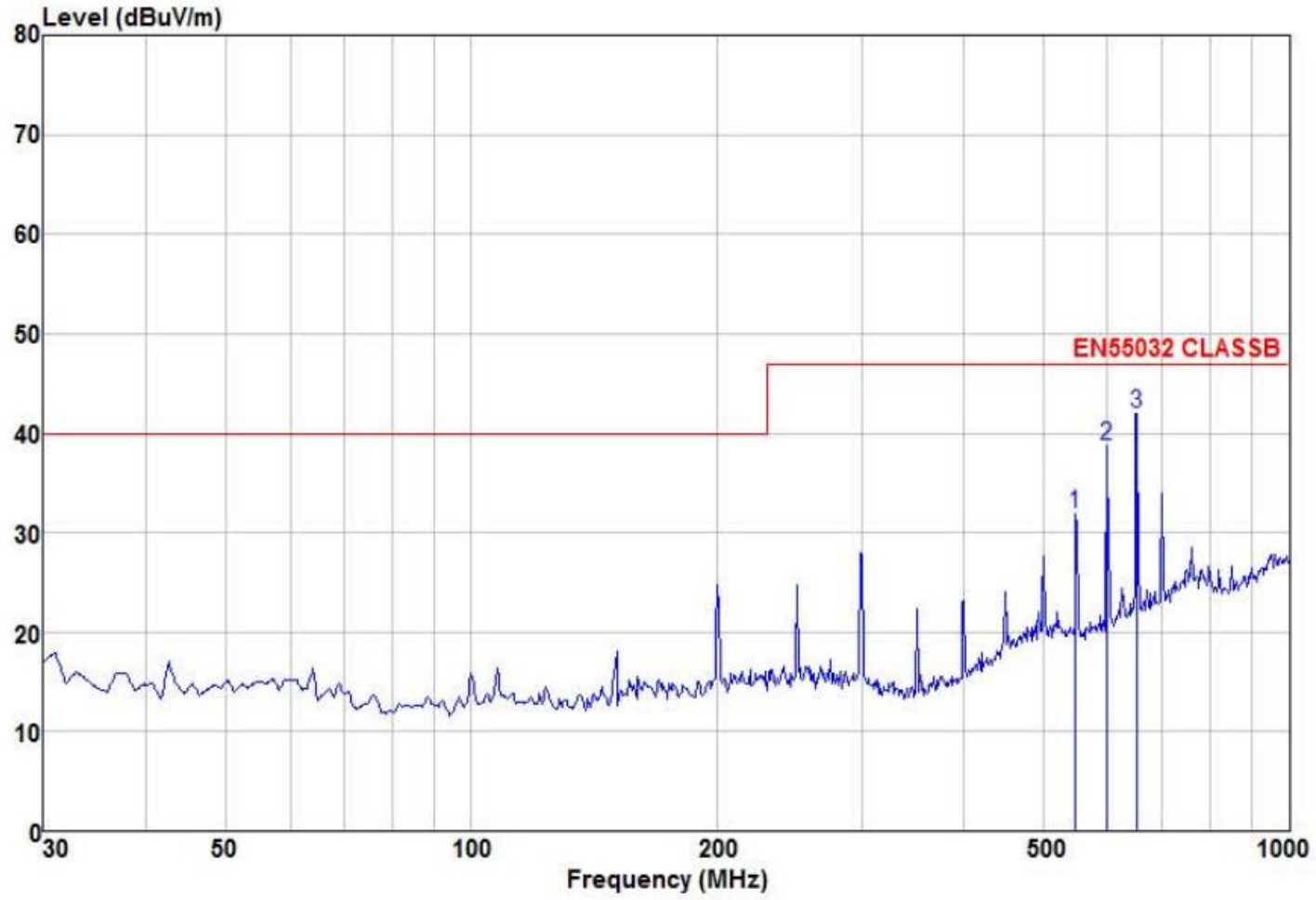

Figure 3-6. Vertical radiation test result

Test conditions:

1) CAN bus load: 5V/180Ω;
2) Secondary-side $VISO_{OUT}$: without additional load.

Test result: 30MHz-1GHz, Margin = 4.95dB

4. Summary

In this application note, we described a low-EMI design of the CA-IS2062A isolated CAN transceivers that uses the ferrite beads, a Y capacitor and differential-mode inductors. This design offers a small size and high-integration solution, while providing respectable electrical performance. The circuit can be built in a relatively small area and optimized to fit a custom footprint.

5. Revision History

Revision Number	Revision Date	Description
Rev 1.0	2024/08/06	Initial version

6. Important Statement

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